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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/735,005	12/12/2000	Kazuyuki Ito	NEC 444	3384

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/735,005	ITO, KAZUYUKI	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-40,42-45,47 and 48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *42-44* is/are allowed.

6)☒ Claim(s) *37-40,45 and 47-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 45 and 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Oyamatsu, US patent No. 5,923,969.

3. Regarding claim 45, Oyamatsu teaches (fig. 13A and 13B) a method of manufacturing a semiconductor device, comprising: defining in a semiconductor substrate (1) first (left hand side of 1) and second (right hand side of 1) element formation regions (region where gate is formed) and an element isolation region (4) isolating the first and second element formation regions from each other; forming first (gate electrode 8 on the left hand side of substrate) and second gate (gate electrode 8 on the right hand side of substrate) electrodes on the first and second element formation regions, respectively; and forming two or more dummy gates (38) over the element isolation region between the first and second gate electrodes (refer to fig. 13B).

4. Regarding claim 47, Oyamatsu teaches the entire claimed process of claim 45 above including each of the dummy gates (38) has a shape that is reduced as compared to the element isolation region (4) (refer to fig. 13B).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37 and 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ukeda et al., US patent No. 6,346,736, admitted prior art (APA) and in view of Inaba et al. US patent No. 6,153,476.

Regarding claim 37 Ukeda teaches (figs. 6a-6h) a method for manufacturing a semiconductor device comprising the steps of: providing a semiconductor substrate (1), forming on the semiconductor substrate, a first photoresist pattern layer using a first photomask having active area patterns corresponding to active areas (6) and dummy area patterns corresponding to dummy areas (9) (Ukeda teaches the use of silicon oxide film 21 and silicon nitride film 22 to form trench structures 14a-14c. The process inherently uses photoresist layer and masking techniques); forming a trench (14a-14c) in the semiconductor substrate (1), which trench partitions pattern areas corresponding to the dummy area patterns (9) from pattern area corresponding to the active area pattern (6), by an etching process using the first photoresist pattern layer as an etching mask, removing the photoresist pattern layer (refer to fig. 6(b)); burying insulating layers (23, figs. 6(c)-6(d)) in the trenches after the photoresist pattern layer is removed; forming a conductive layer (4, 51 and 10) over the semiconductor substrate (1) forming a second photoresist pattern layer (refer to col. 17, lines 14-21) on the conductive layer

using a second photomask having gate pattern (4) corresponding to the active area (6) and dummy gate patterns (51) corresponding to the dummy areas (9) and patterning the conductive layer by an etching process using the second photoresist pattern layer; each of the dummy gate pattern having a reduced area of the respective one of the dummy area patterns (the dummy gate pattern 51 has an area that is smaller than the dummy area pattern below it (area defined by 9 and the isolation 14b), that means the surface area of the region below the dummy gate 51 is larger than the surface area of the dummy gate area 51).

Ukeda does not explicitly teach forming more than one active area patterns, more than one gate patterns, more than one dummy gate patterns, forming an isolation layer on the semiconductor substrate, the gate patterns and the trenches; perforating contact holes in the isolation layer: and forming a connection layer on the isolation layer and connecting the connection layer via the contact holes to the semiconductor substrate.

However it is conventional and also taught by APA forming more than one (fig. 3c) gate patterns (P1) and dummy patterns (DP) on a semiconductor substrate (201).

Furthermore forming contact holes to form connection to a semiconductor device is conventional in the art and also taught by Inaba (figs. 3B-3C) where an isolation layer (31) is formed on a semiconductor substrate (11), the gate patterns (21B, 21A) and trenches (12); perforating contact holes (32A) in the isolation layer (31): and forming a connection layer (33) on the isolation layer (31) and connecting the connection layer via the contact holes to the semiconductor substrate (11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the plurality of dummy gate patterns and gate patterns taught by APA in the process of Ukeda in order to make a semiconductor device that requires the formation of a plurality gate structures and a plurality dummy gate structures. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of forming interconnection structure taught by Inaba in the combined process of Ukeda and APA in order to further integrate the device.

Regarding claim 39, Ukeda teaches substantially the entire claimed method of claim 37 above including the dummy gates (DP, refer to APA) are arranged in at least two rows (refer to fig. 3C, APA).

Regarding claim 40, Ukeda teaches substantially the entire claimed method of claim 37 above including at least one said row is shifted from another said row (refer to APA fig. 3C, the spacing between the rows are not the same).

6. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ukeda, Inaba, APA and in view of Shimomura et al. US patent No. 6,140,687.

Regarding claim 38 Ukeda teaches substantially the entire claimed method of claim 37 above except explicitly stating that the shape of the dummy area and/ or dummy gate is a circle.

It is conventional and also taught by Shimomura forming circular shaped gates.

It would be well within one of ordinary skill in the art to select circular shape dummy/gate structures since circular structures allow for symmetrical arrangement of integrated circuit layout. Furthermore since it is known to form circular shaped gate electrodes it would have been obvious to form circular dummy gate electrode.

7. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ukeda, APA and in view of Kurosawa, US patent No. 4,866,494.

Regarding claim 48 Ukeda teaches substantially the entire claimed method of claim 37 above except explicitly stating that the trench is grid shaped.

However grid-shaped trenches are conventional in the art and also taught by Kurosawa in a process of forming a memory device (refer to fig. 2, and col. 3, lines 57-69) where the trench structure is grid shaped.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the grid shaped trench structure taught by Kurosawa in the process of Ukeda in order to provide better isolation.

Allowance

8. Claims 42-44 are allowed.

Reason for allowance

9. The following is an examiner's statement of reasons for allowance: The prior art of record does not teach or suggest, singularly or in combination at least the limitation "performing a selective etching on a semiconductor substrate having first and second active areas and an isolation area intervening between the first and second active areas, thereby forming a grid-shaped trench in the isolation area of the semiconductor

substrate to define a plurality of dummy regions each surrounded by the grid-shaped trench; where the dummy gate having a reduced shape area as compared to shape area of the corresponding of said dummy regions" as recited in claim 42.

Response to Arguments

10. Applicant's arguments with regards to claims 37-40, filed 6/23/2005 have been fully considered but they are moot in view of new grounds of rejection. With regards to applicant arguments to claims 45 and 47, the limitation of forming first and second gate electrodes on the first and second element formation region and forming two or more dummy gates on the element isolation region between the first and second gate electrodes is clearly taught by Oyamatsu teaches (fig. 13A and 13B).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Loke can be reached on (571) 272-1657. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
September 19, 2005

Steven Loke